

Fig. 1

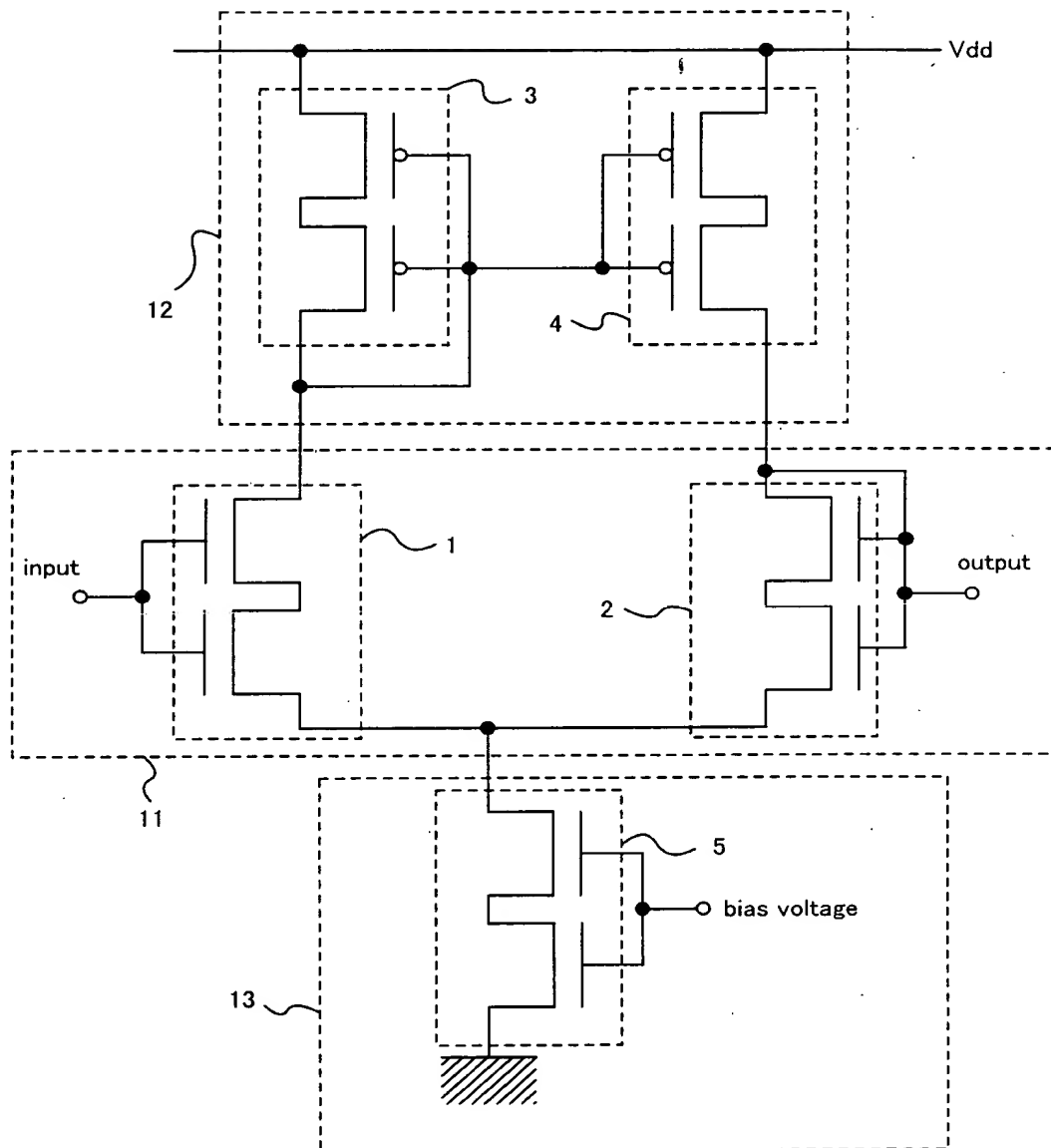


Fig. 2

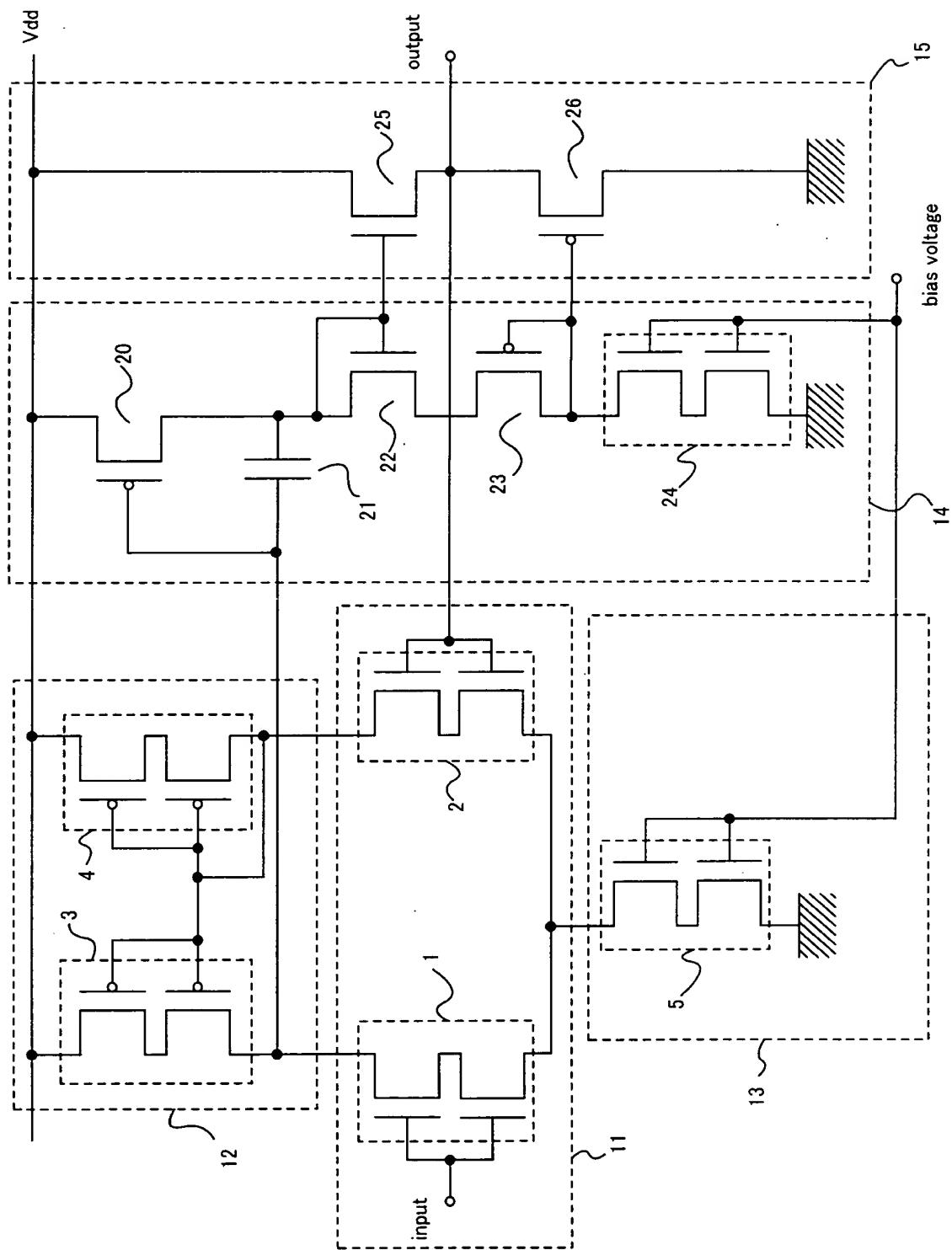
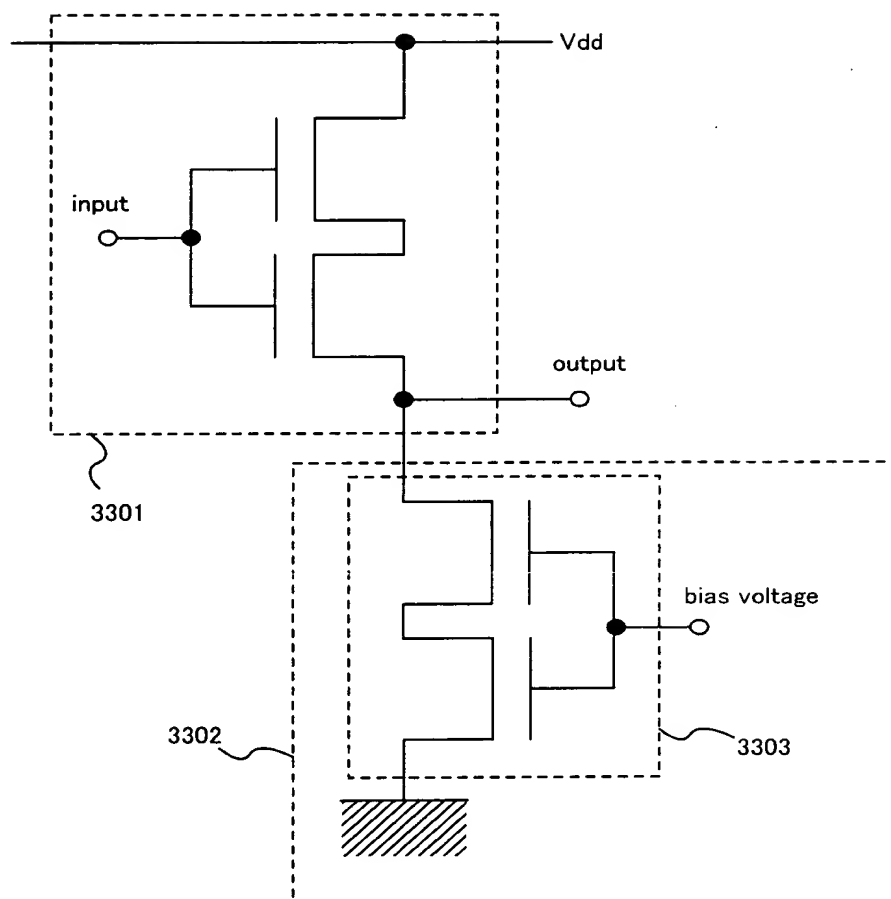
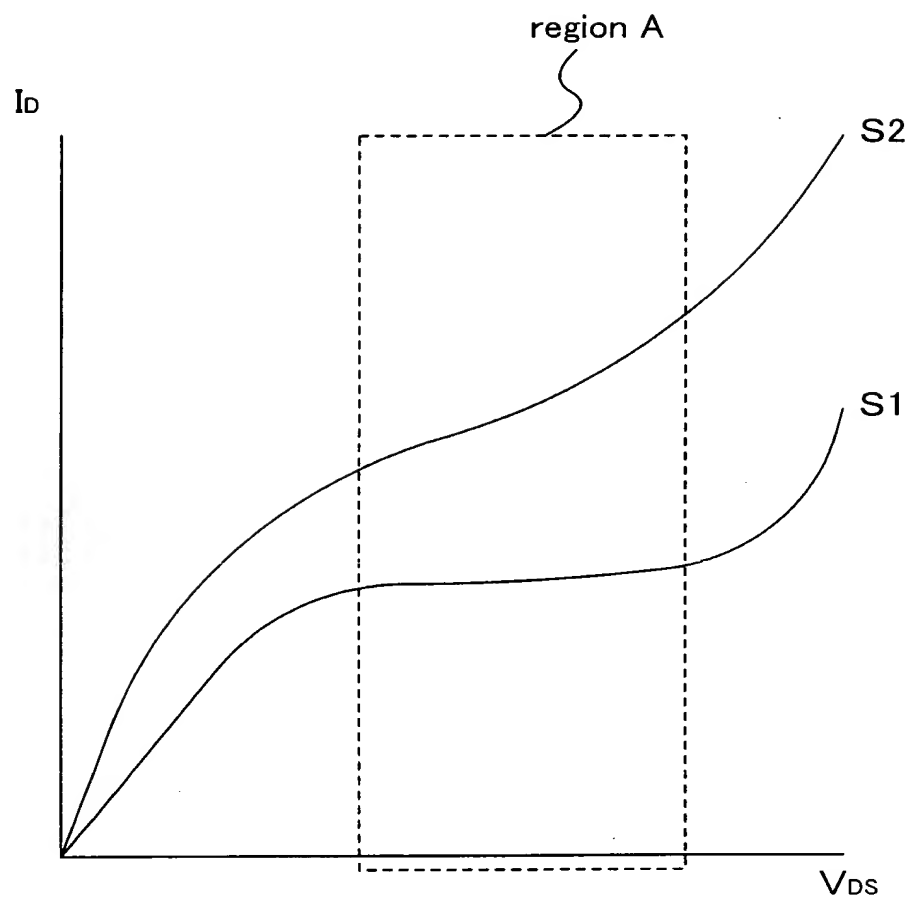


Fig. 3



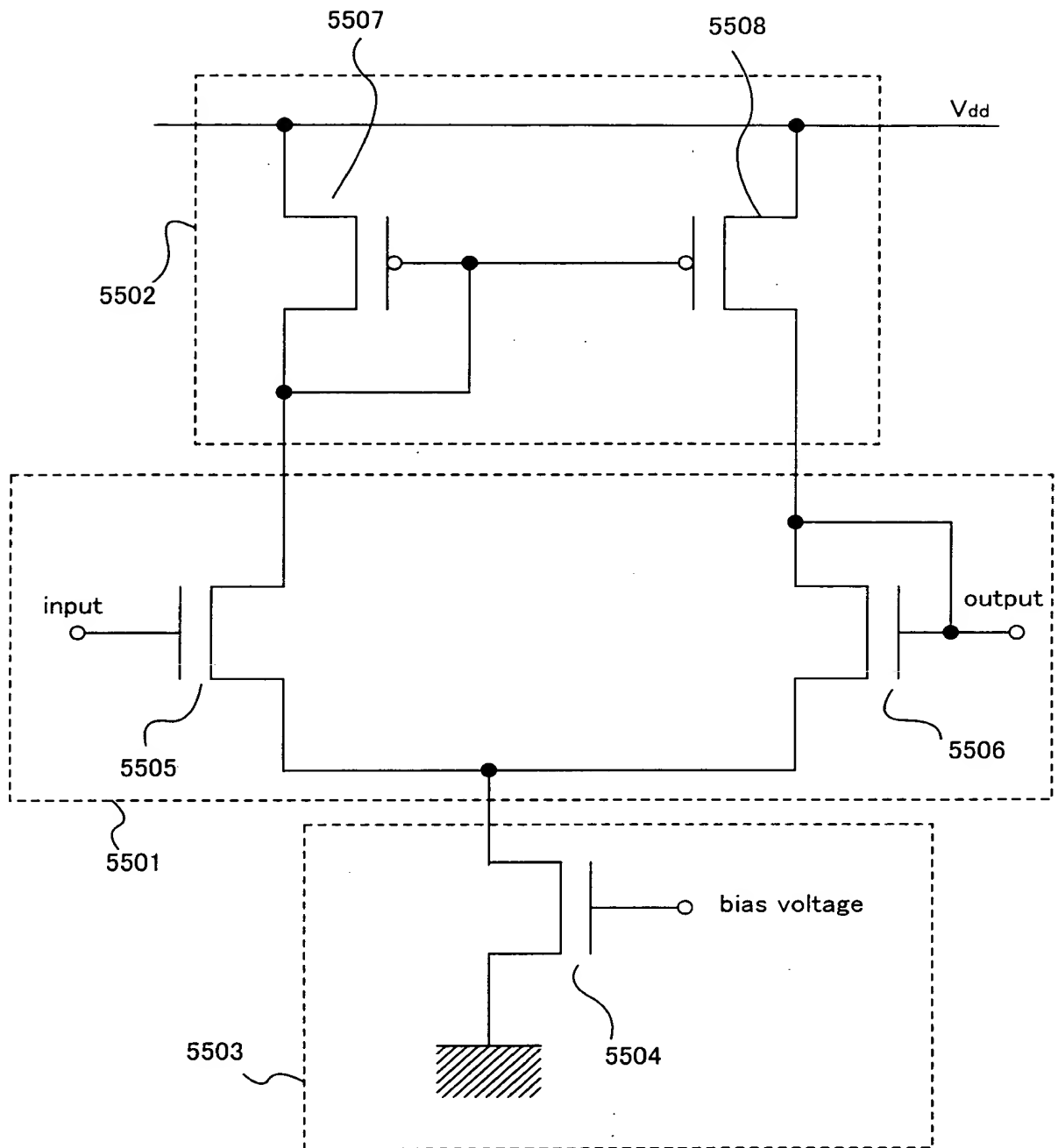
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Fig. 4



Prior

Fig. 5



0986743-1004

Fig. 6

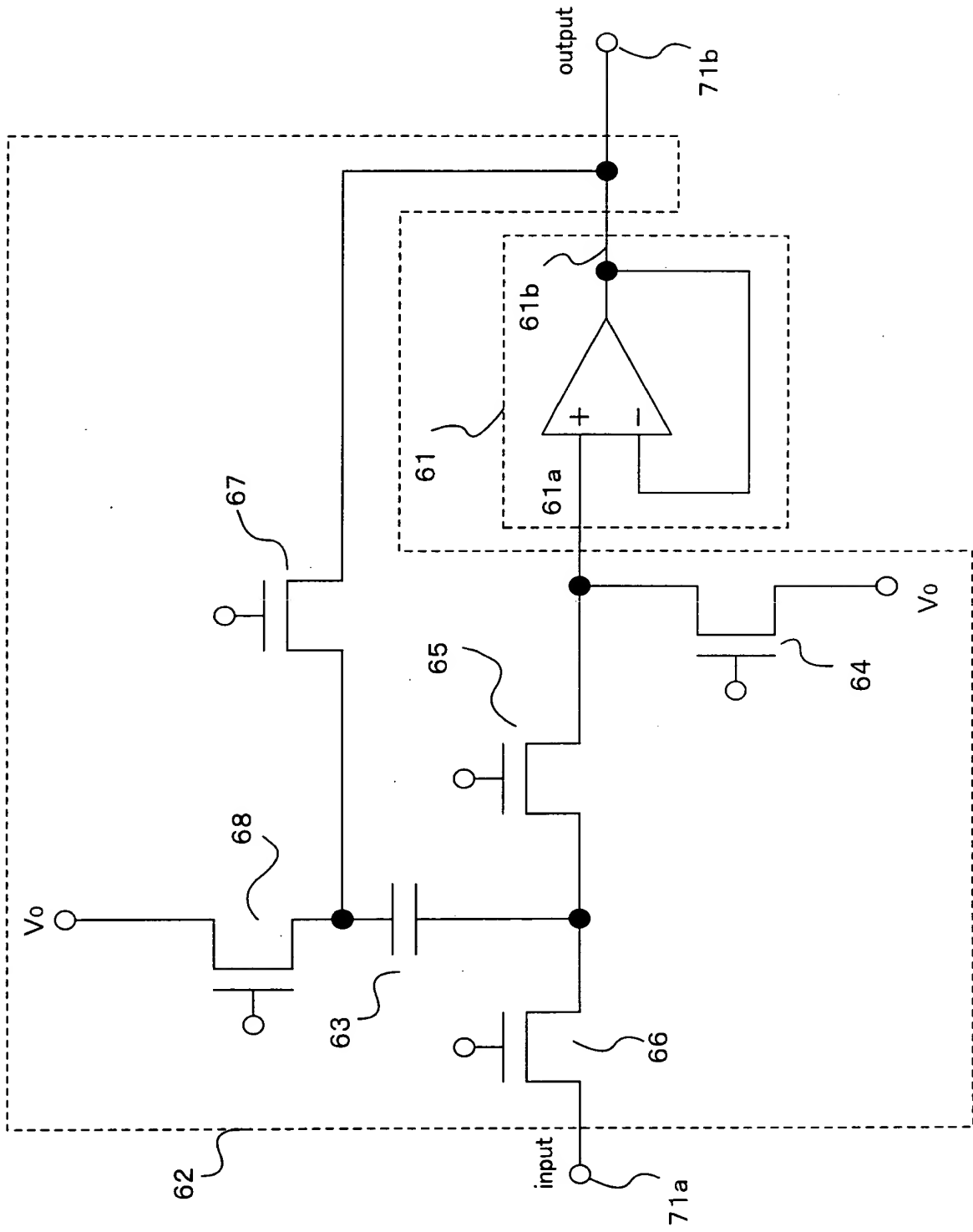


Fig. 7

Prior

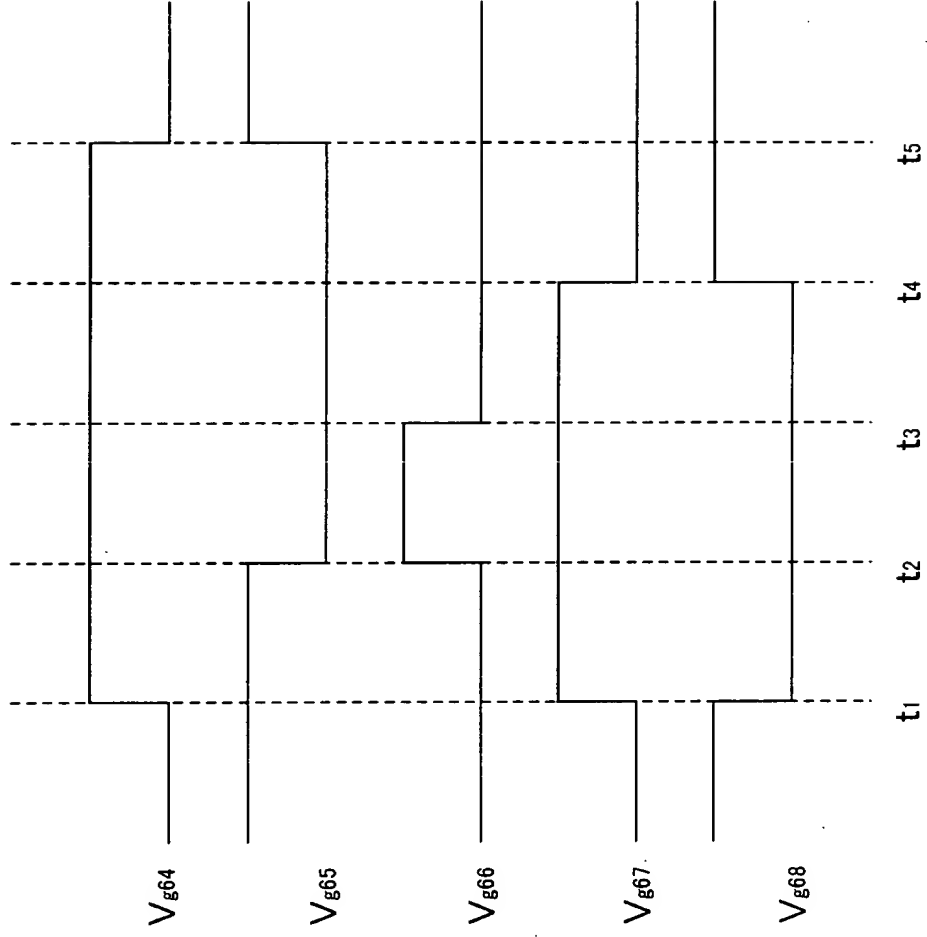
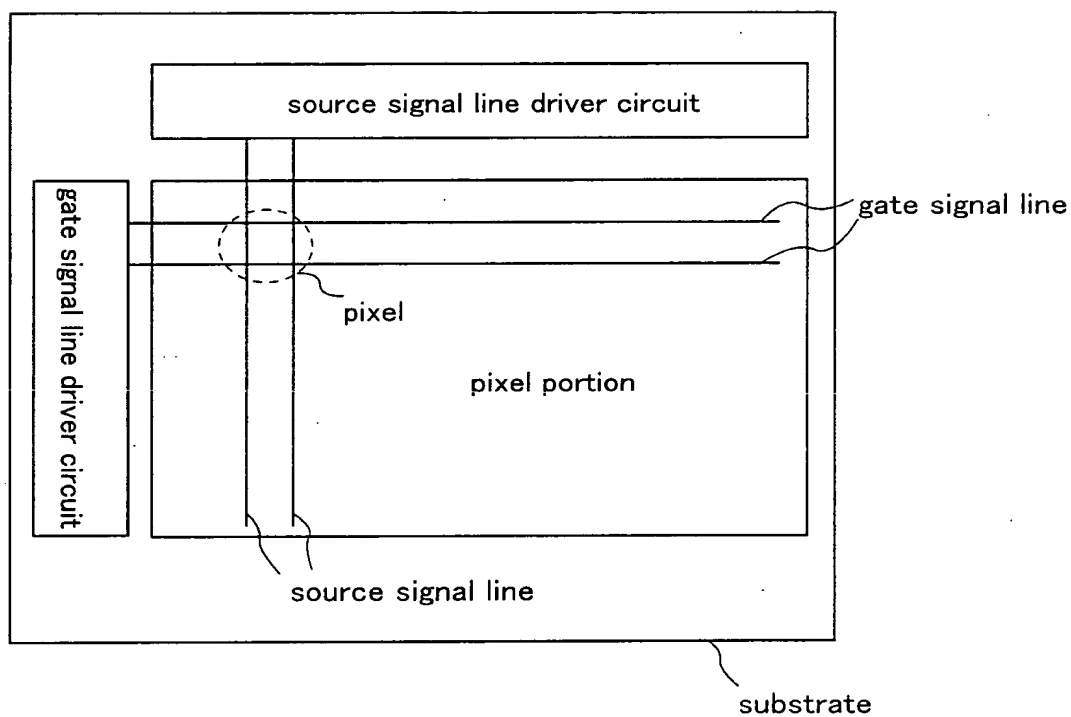


Fig. 8



09586742.10901

Fig. 9

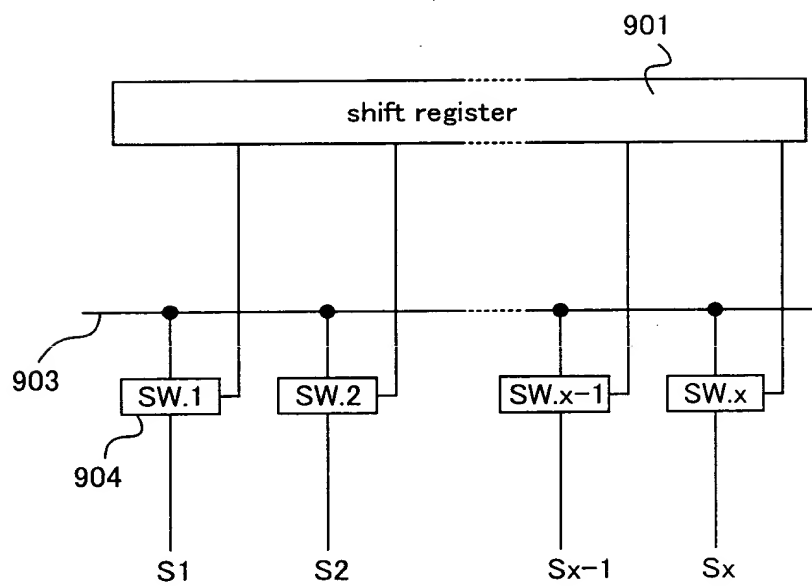


Fig. 10

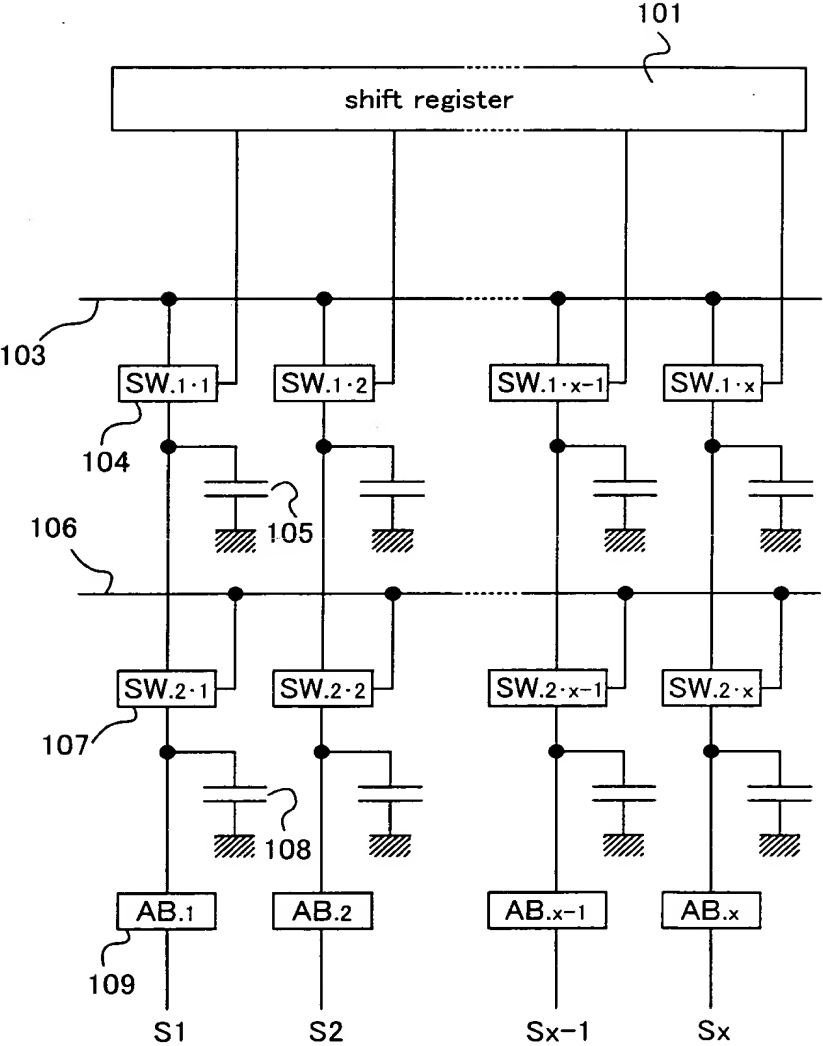


FIG. 10

Fig. 11A

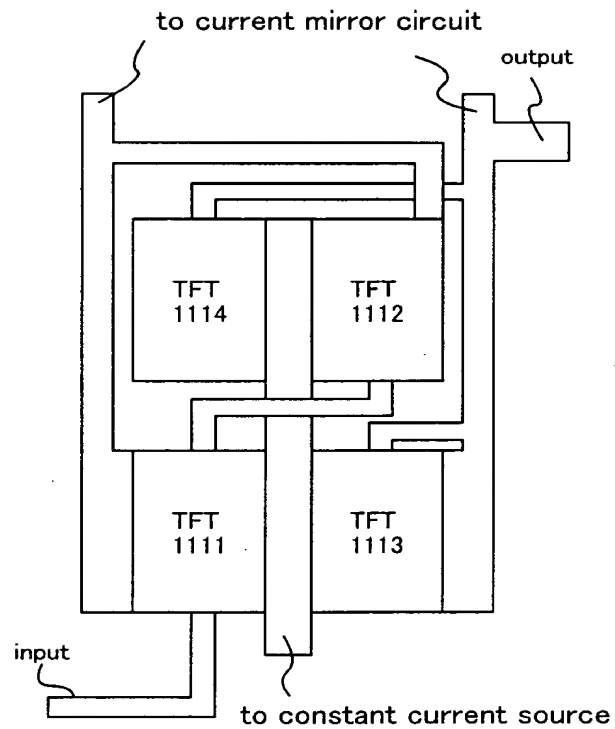


Fig. 11B

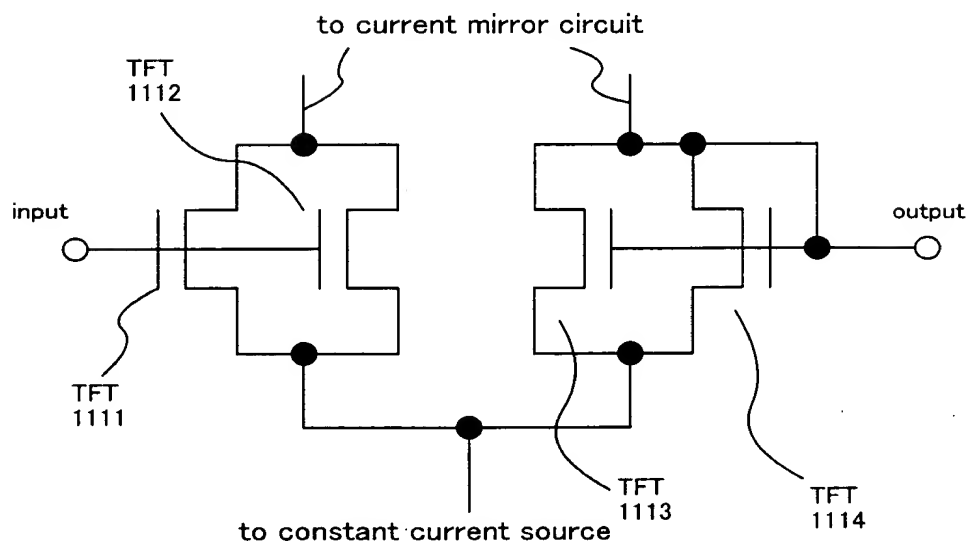


Fig. 12

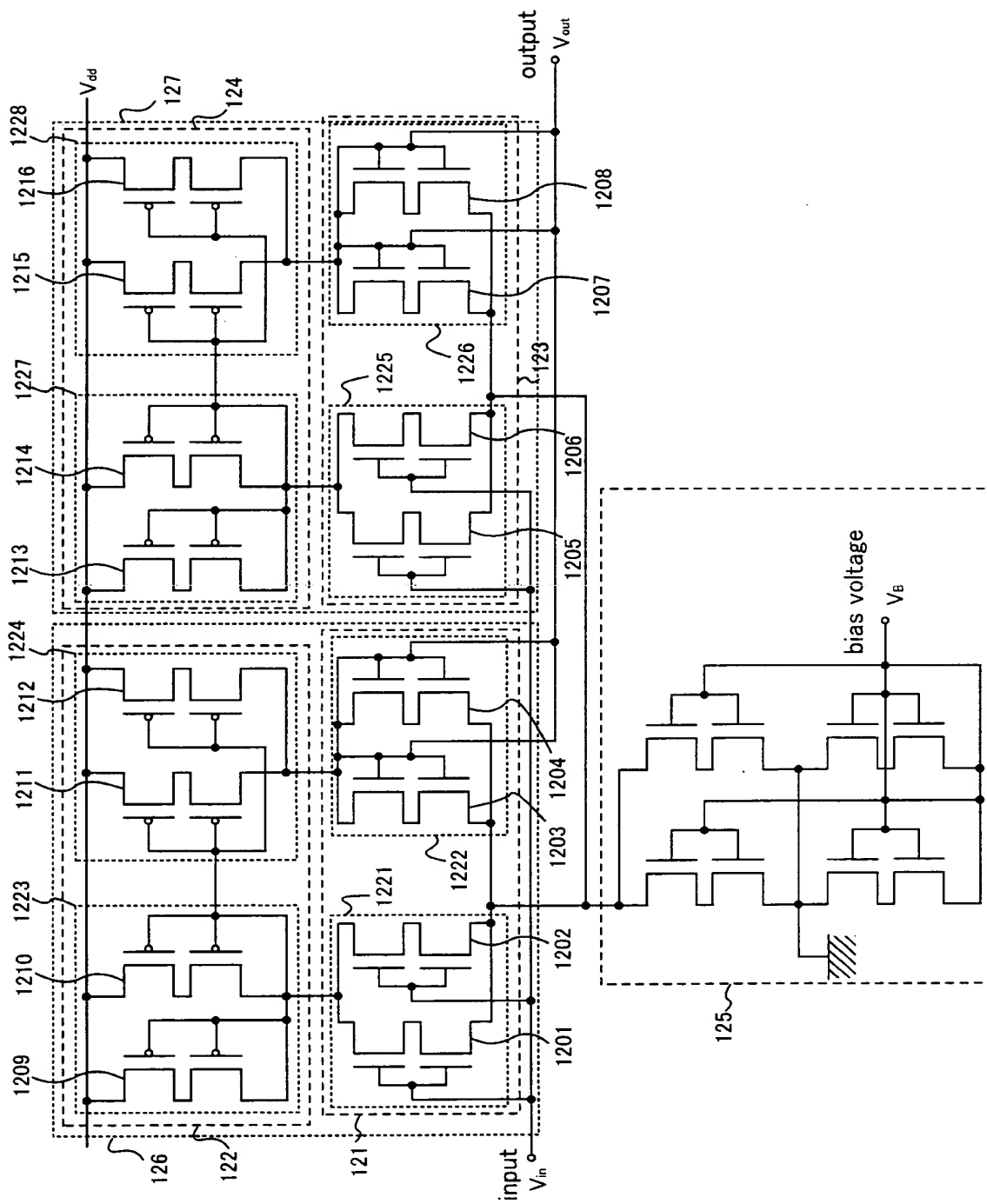


Fig. 13

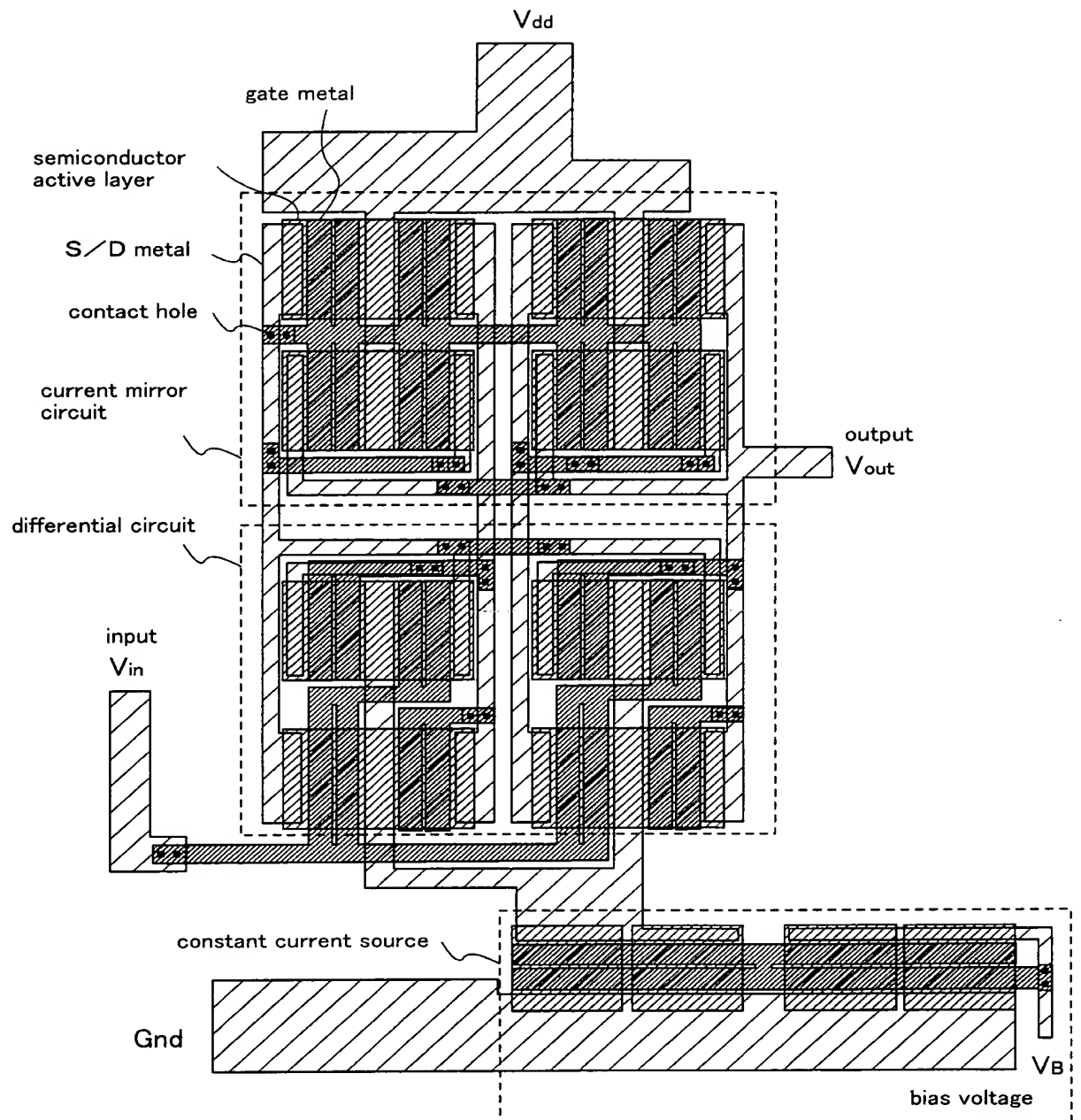
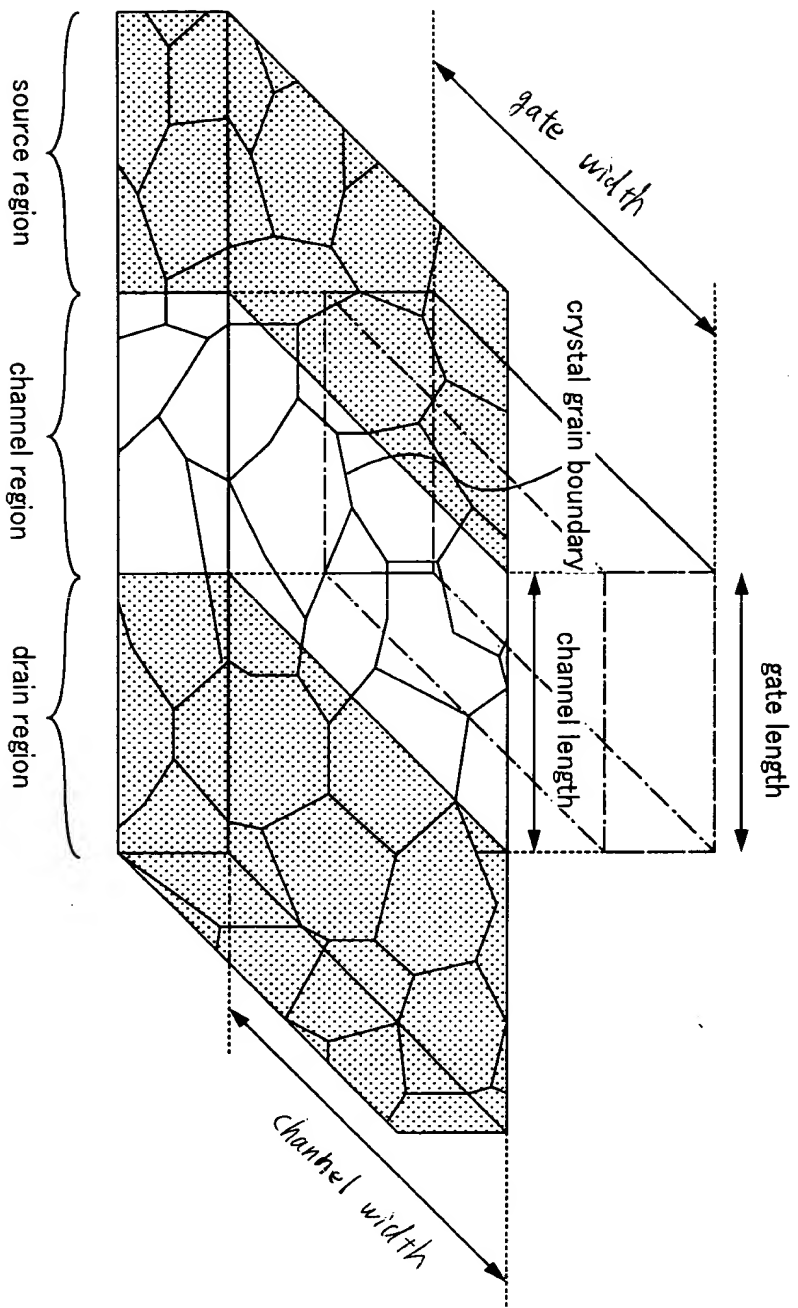


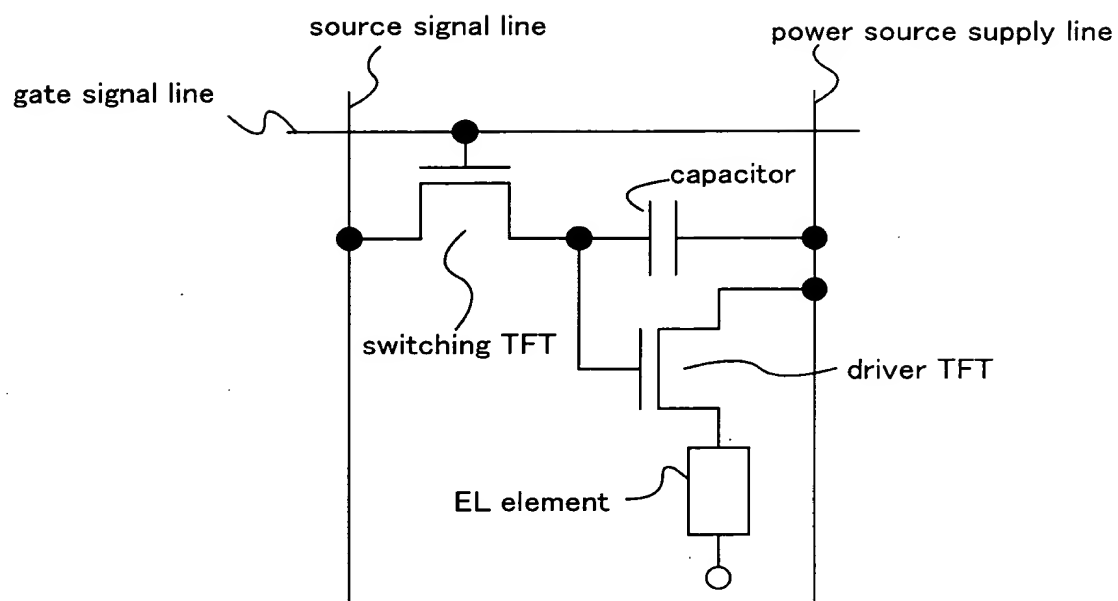
FIG. 13

Fig. 14



09986742.110901

Fig. 15



09986742 110901

Fig. 16A

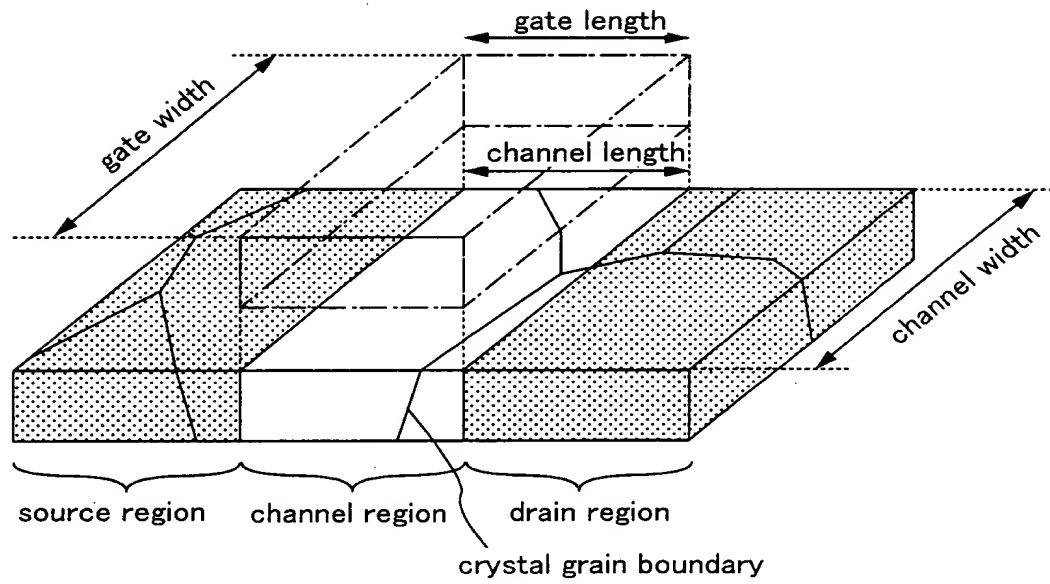


Fig. 16B

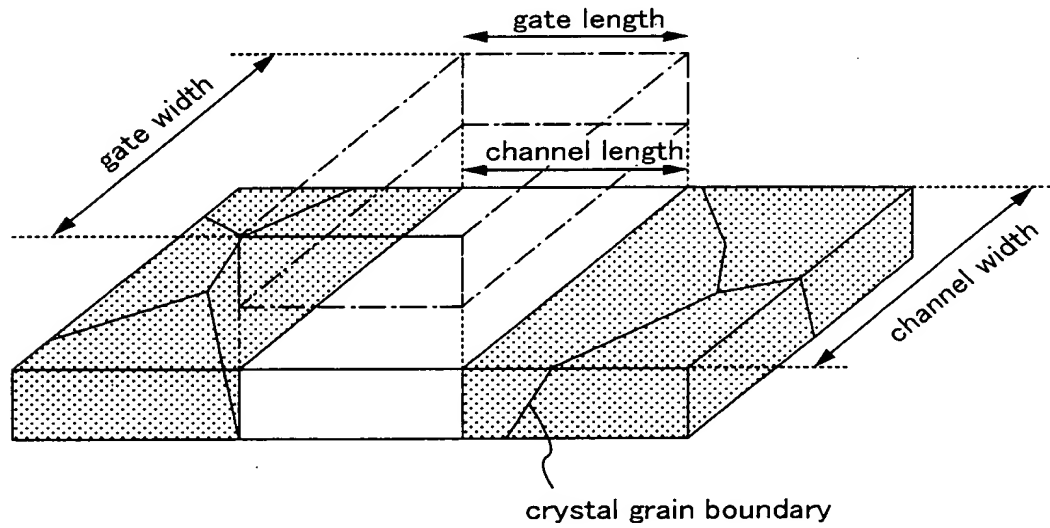


Fig. 17

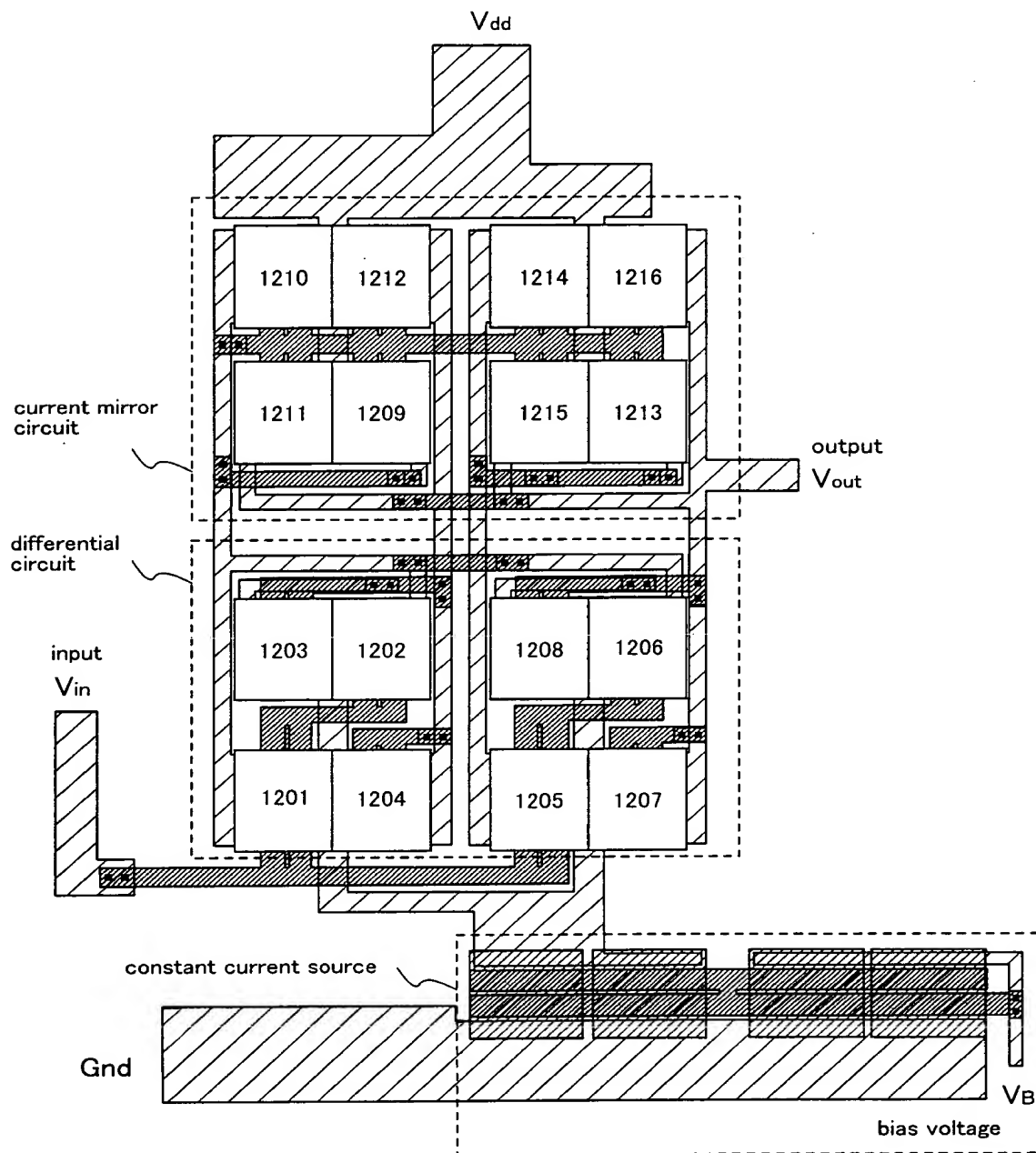


Fig. 18

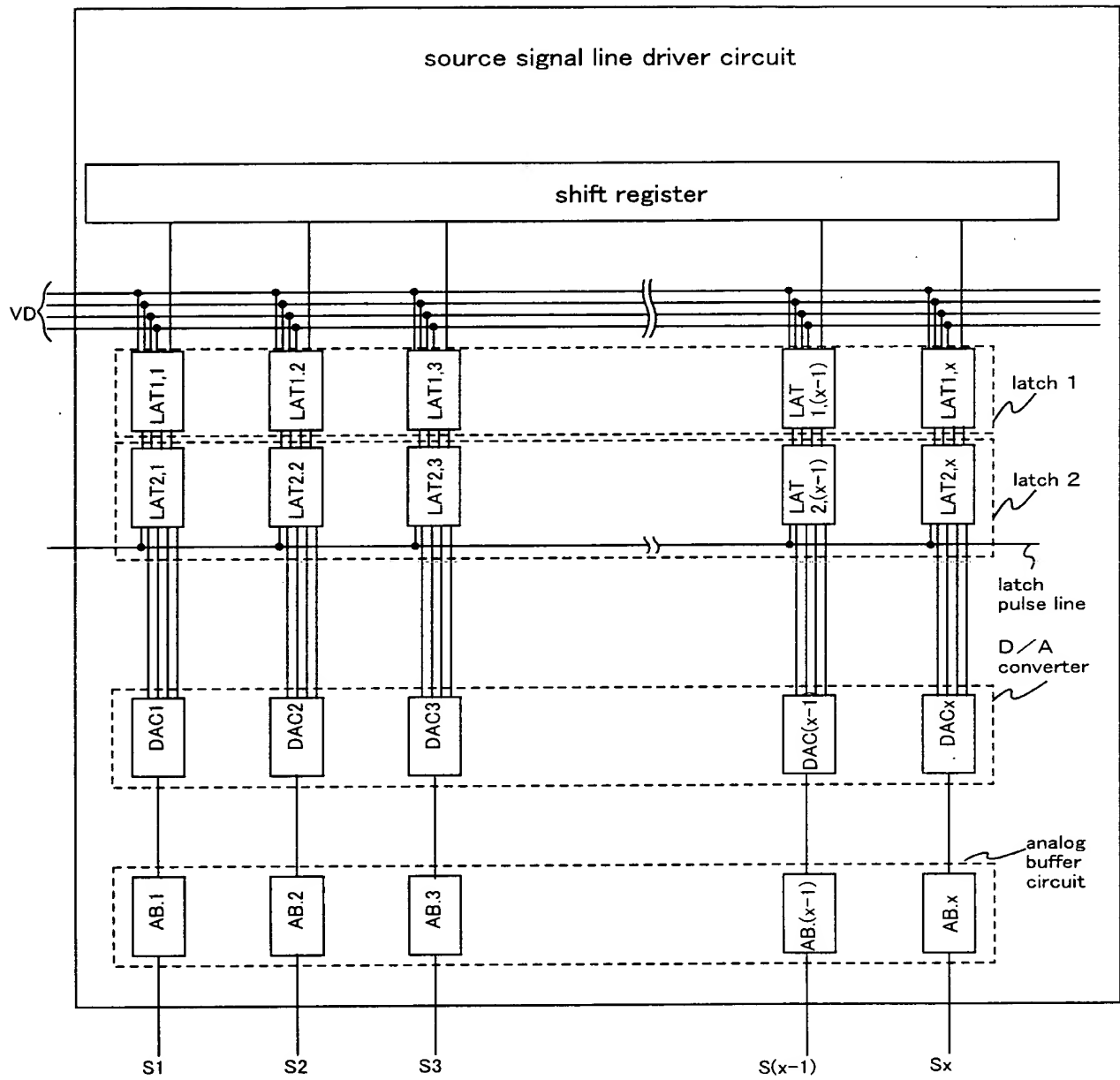


Fig. 19A

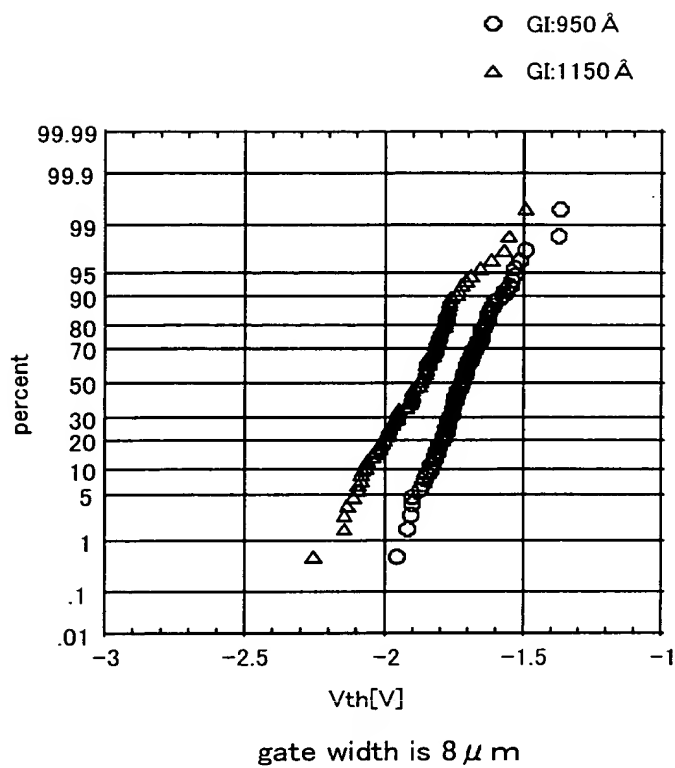
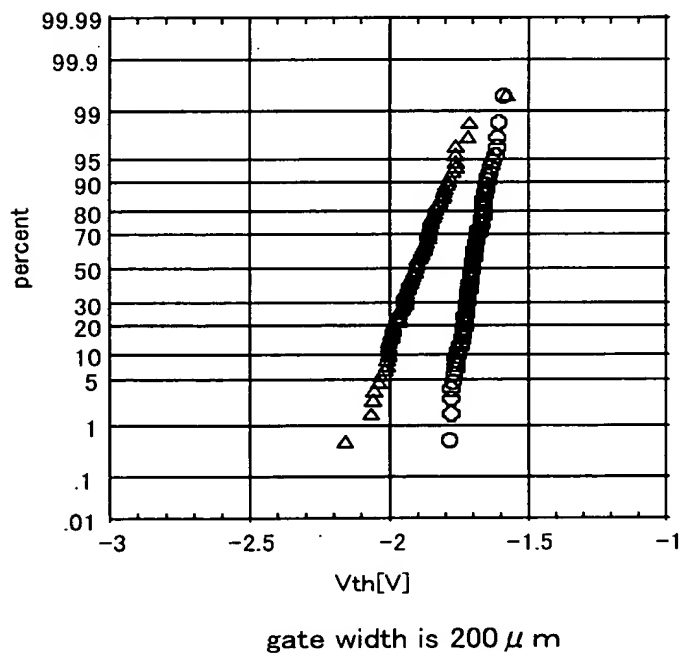


Fig. 19B



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Fig. 20A characteristic of input and output in buffer circuit

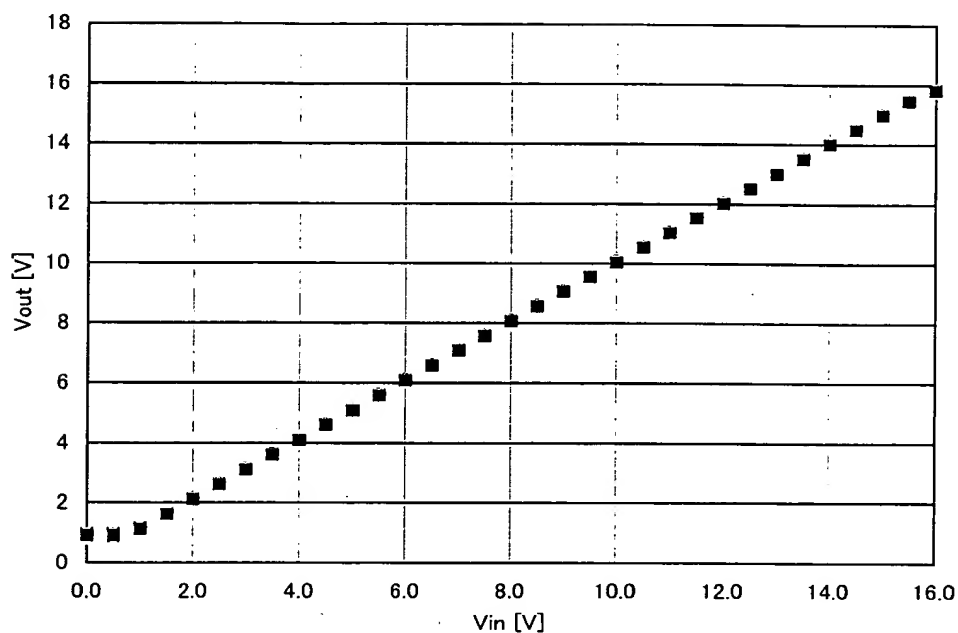


Fig. 20B

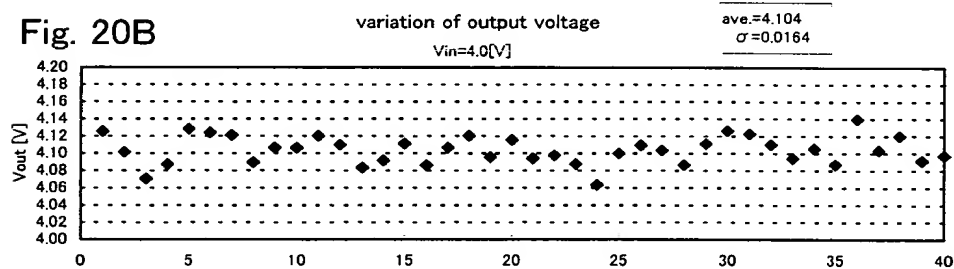


Fig. 20C

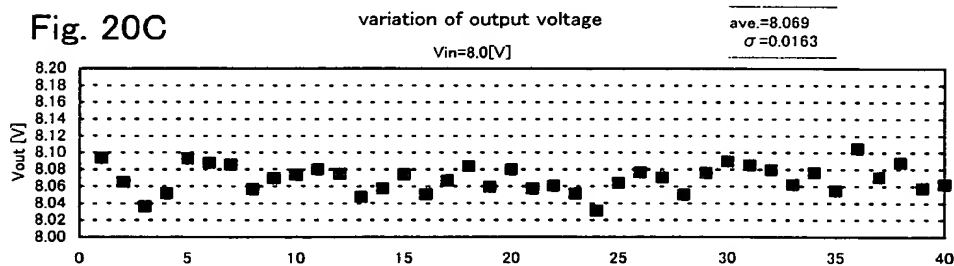


Fig. 20D

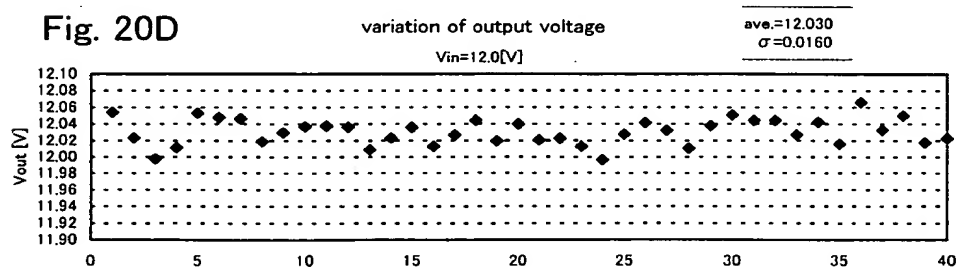


Fig. 21A semiconductor layer formation/insulating film formation/formation of first and second conductive films

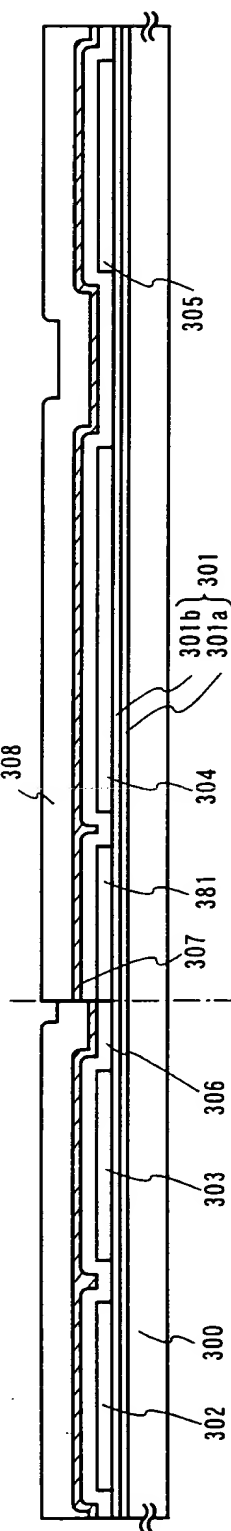


Fig. 21B first etching process/first doping process

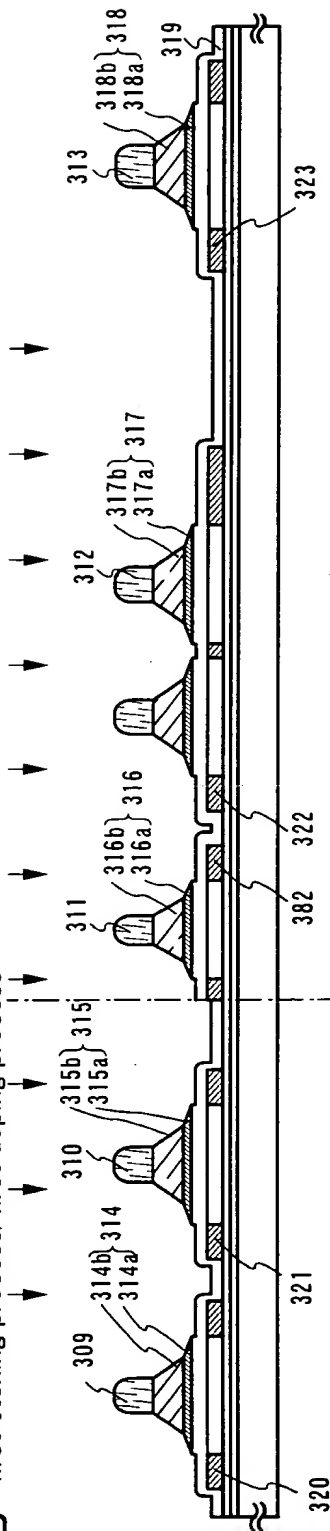


Fig. 21C second etching process

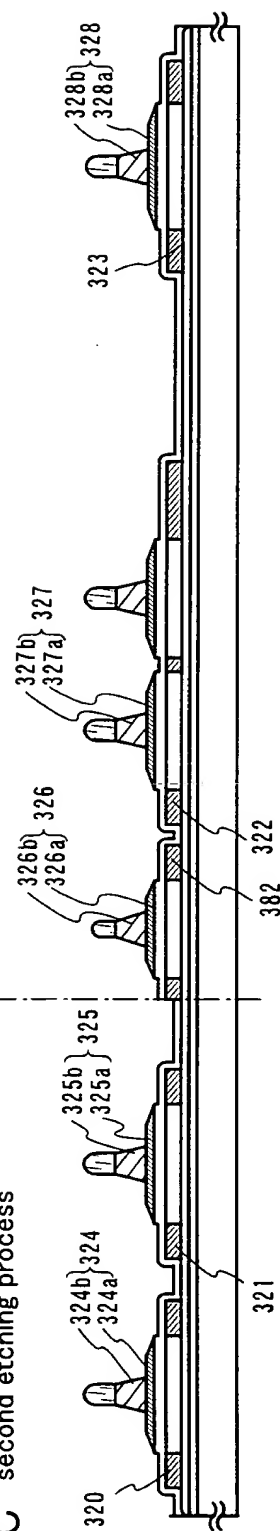


Fig. 22A second doping process

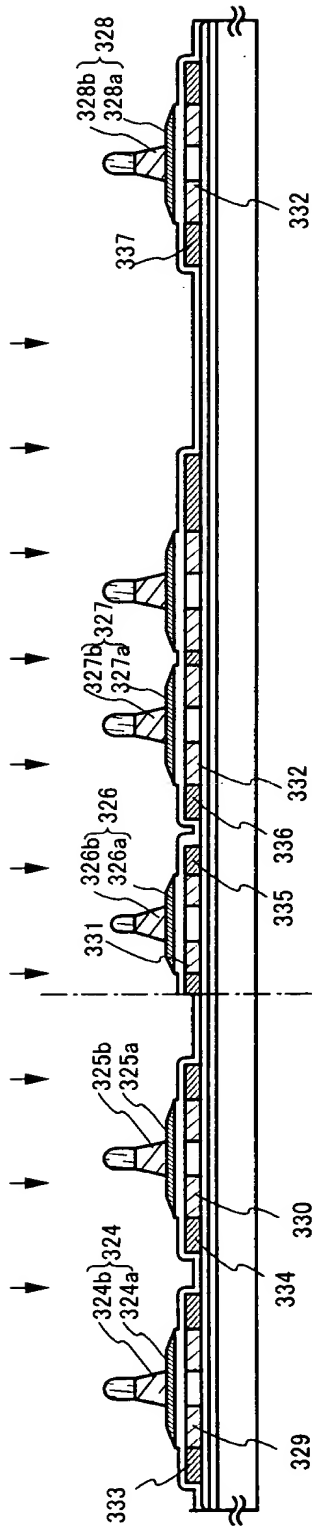


Fig. 22B third etching process

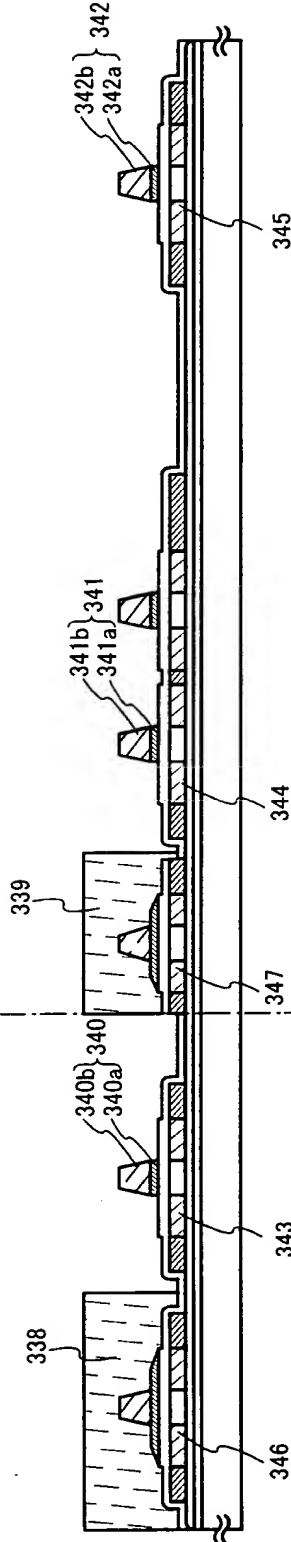


Fig. 22C third doping process

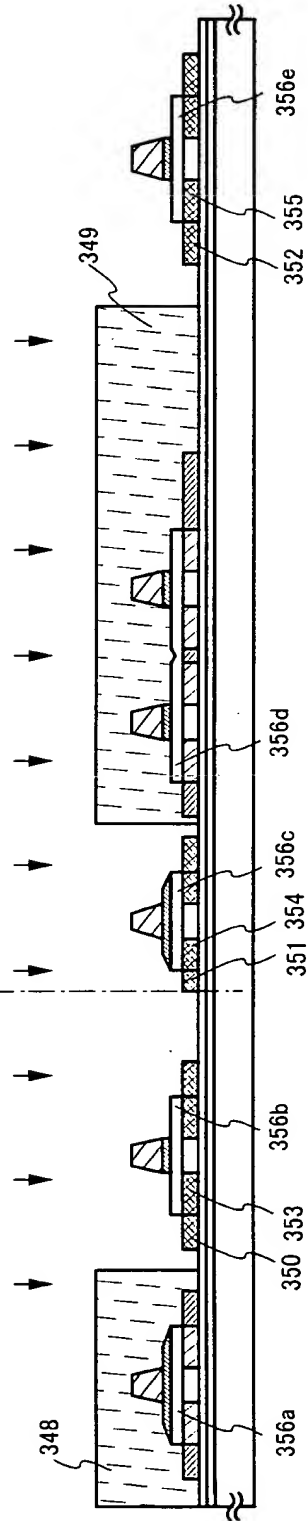


Fig. 23A formation of first interlayer insulating film, activating process

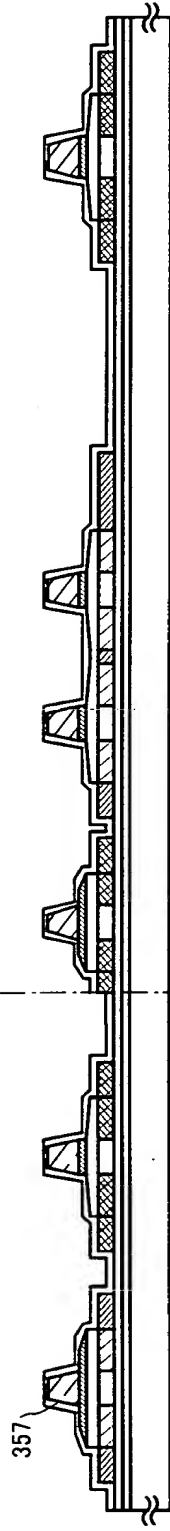


Fig. 23B formation of second interlayer insulating film, wiring, pixel electrode

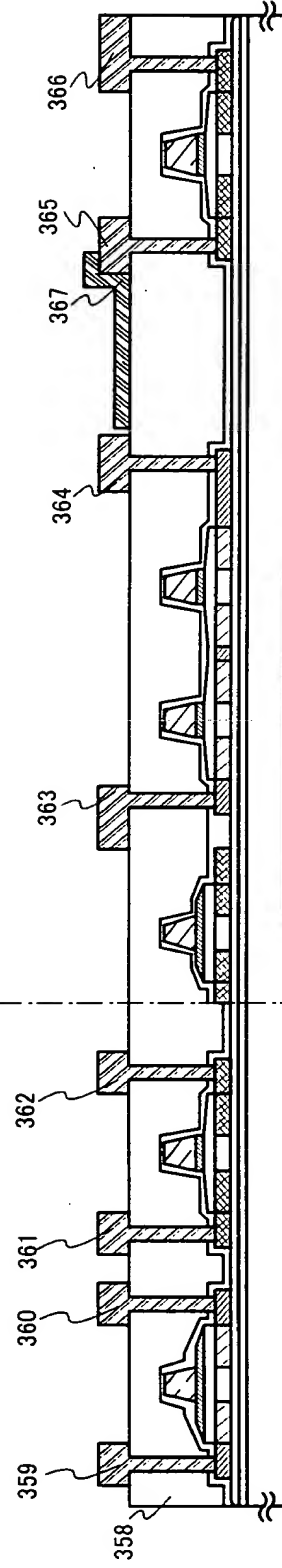
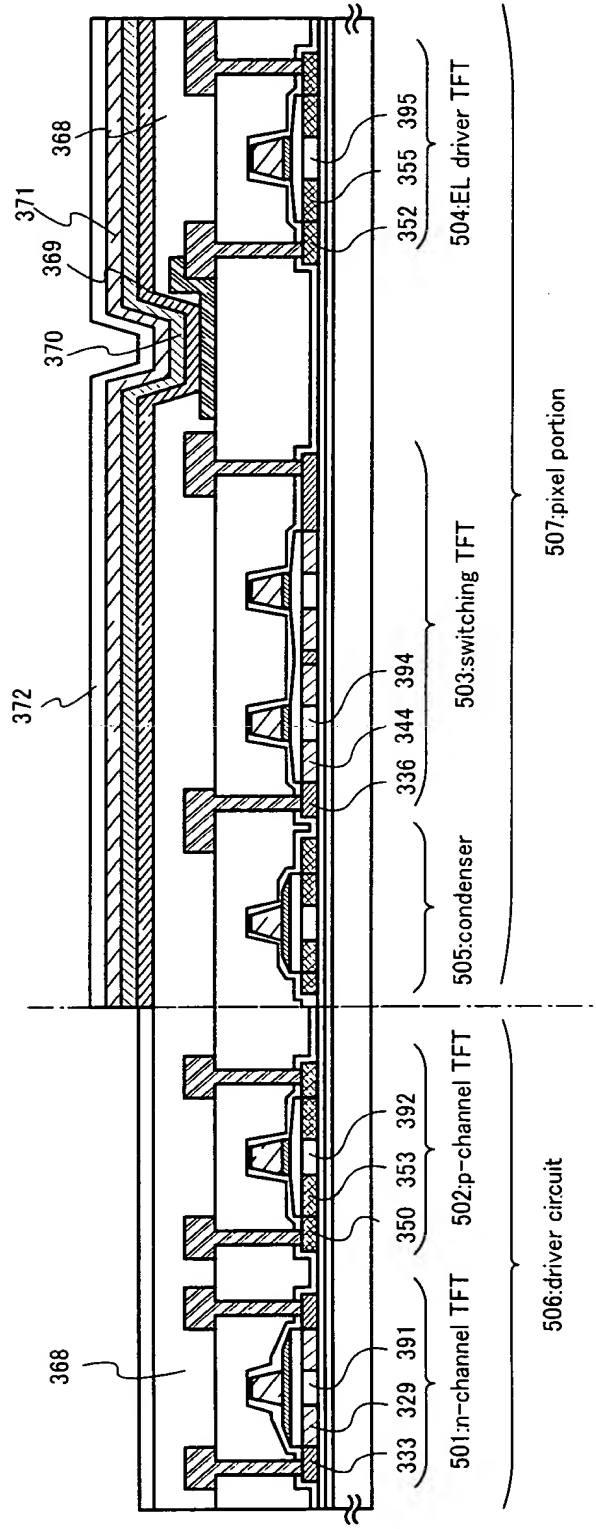


Fig. 24 formation of third interlayer insulating film, EL layer, pixel electrode, passivation film



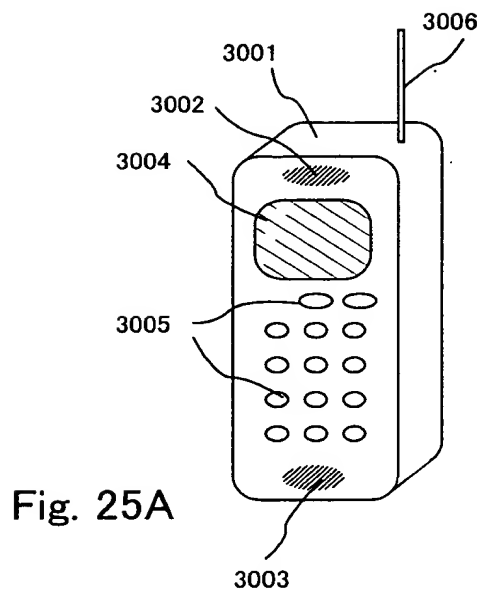


Fig. 25A

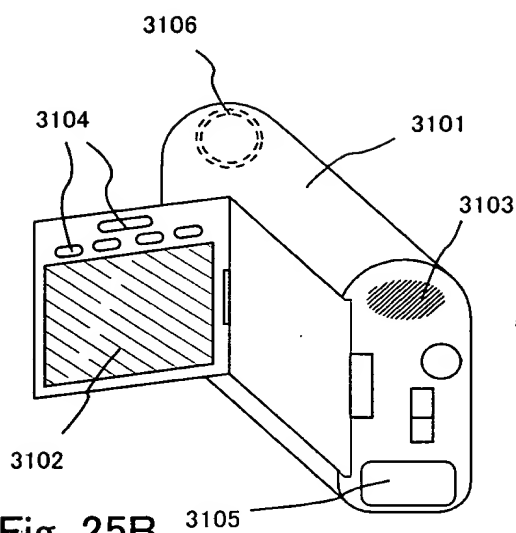


Fig. 25B

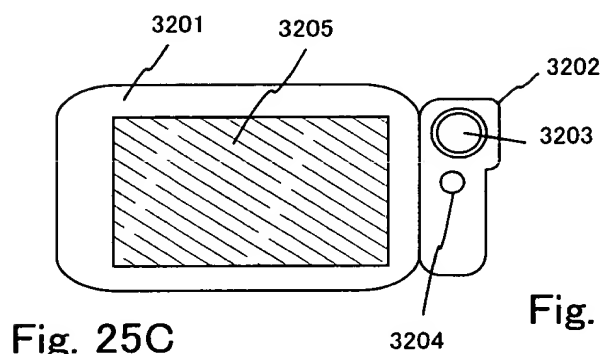


Fig. 25C

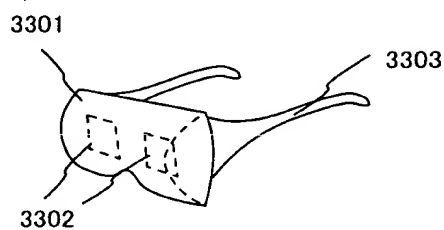


Fig. 25D

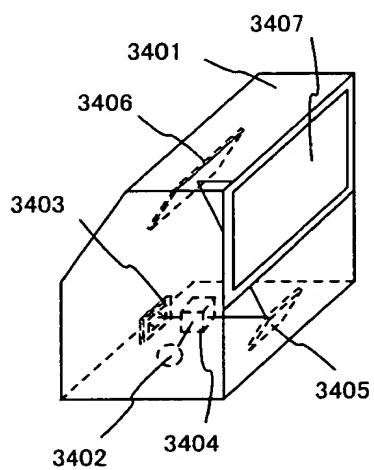


Fig. 25E

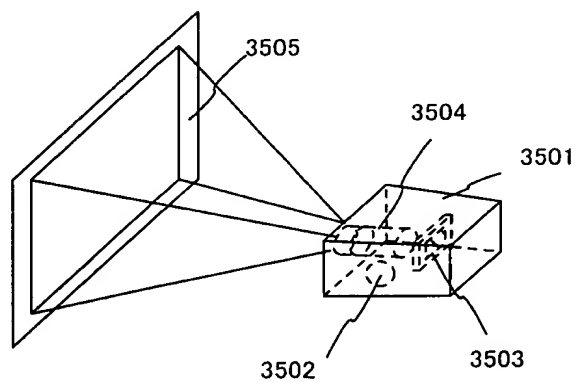


Fig. 25F